MULTIMEDIA UNIVERSITY ™

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 1, **2018/2019**

EEE 3156 DIGITAL SYSTEM

(EE Group)

18 OCTOBER 2018

2:30 PM – 4:30 PM
(2 Hours)

INSTRUCTION TO STUDENT

1. This Question paper consists of 4 pages including cover page with 4 Questions only.

2. Attempt **ALL FOUR** questions. All questions carry equal marks and the distribution of the marks for each question is given.

3. Please print all your answers in the Answer Booklet provided.

Question 1:

(a) Generate the truth table for the following equations.

$F1 = \bar{A}\,\bar{B}\,\bar{C} + \bar{A}\,\bar{B}\,C\,\bar{D} + (\bar{A}\,B + AB)D + ABC\bar{D} + A\bar{B}\,\bar{D}$

$F2 = \bar{A}\,\bar{B} + \bar{A}\,BD + ABCD + A\bar{B}\,\bar{C} + A\bar{B}C\,\bar{D}$

[4 marks]

(b) Compute the simplified characteristic equations of F1 and F2 from part (a).

[8 marks]

(c) From part (b), design the functions F1 and F2 using:-

(i) Standard logic gates only.

[6 marks]

(ii) Pure NAND gates only.

[7 marks]

Question 2:

(a) Design the single bit Logic Circuit shown in Table Q2 using standard logic gates and multiplexer.

Table Q2

S_1S_0	Logic Operation
00	$F = \bar{A}$
01	F = AB
10	F = A + B
11	$F = A \oplus B$

[5 marks]

(b) Create the truth table and compute the simplified characteristic equation of function, F for the logic circuit shown in part (a).

[9 marks]

(c) From part (a), design the Logic Circuit using:-

(i) Programmable logic arrays only.

[6 marks]

(ii) One unit look up table only.

[5 marks]

Continued ...

Question 3:

(a) Create the state assigned table of the system shown in Figure Q3. Given that W = input signal and Z = output signal.

[4 marks]

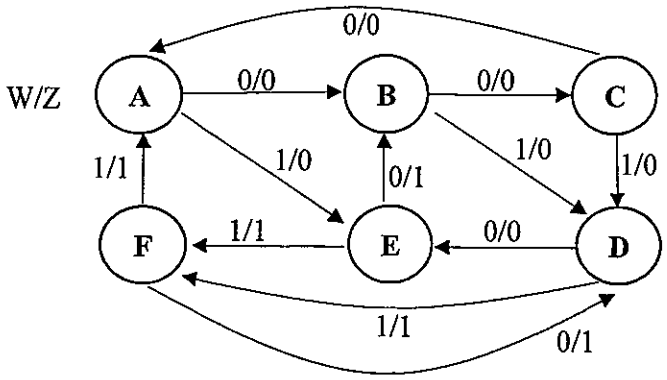

Figure Q3

(b) Compute the simplified characteristic equations for the next state signals and output signal of the system shown in Figure Q3.

[12 marks]

(c) Design the system shown in Figure Q3 using programmable logic array and D flip-flops.

[9 marks]

Continued ...

Question 4:

(a) Create the truth table of a single bit full adder.

[4 marks]

(b) Compute the characteristic equations of the single bit full adder.

[9 marks]

(c) Refer to Table Q4, design a single bit arithmetic circuit of the n-bit Parallel Adder as shown in Figure Q4 using the standard logic gates.

[5 marks]

Table Q4

S_1S_0	Y=	Cin=0	Cin=1
00	0	G = A	G = A plus 1
01	B	G = A plus B	G = A plus B plus 1
10	B'	G = A plus B'	G = A minus B
11	1	G = A minus 1	G = A

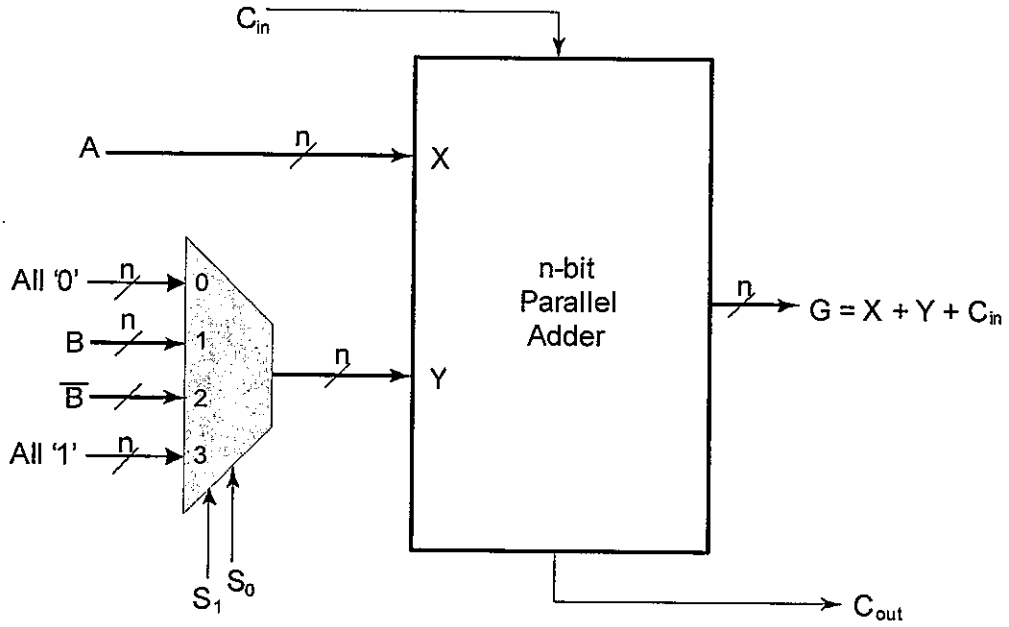

Figure Q4

(d) Design a single bit circuit to generate signal, Y in Figure Q4 using standard logic gates.

[7 marks]

End of Paper